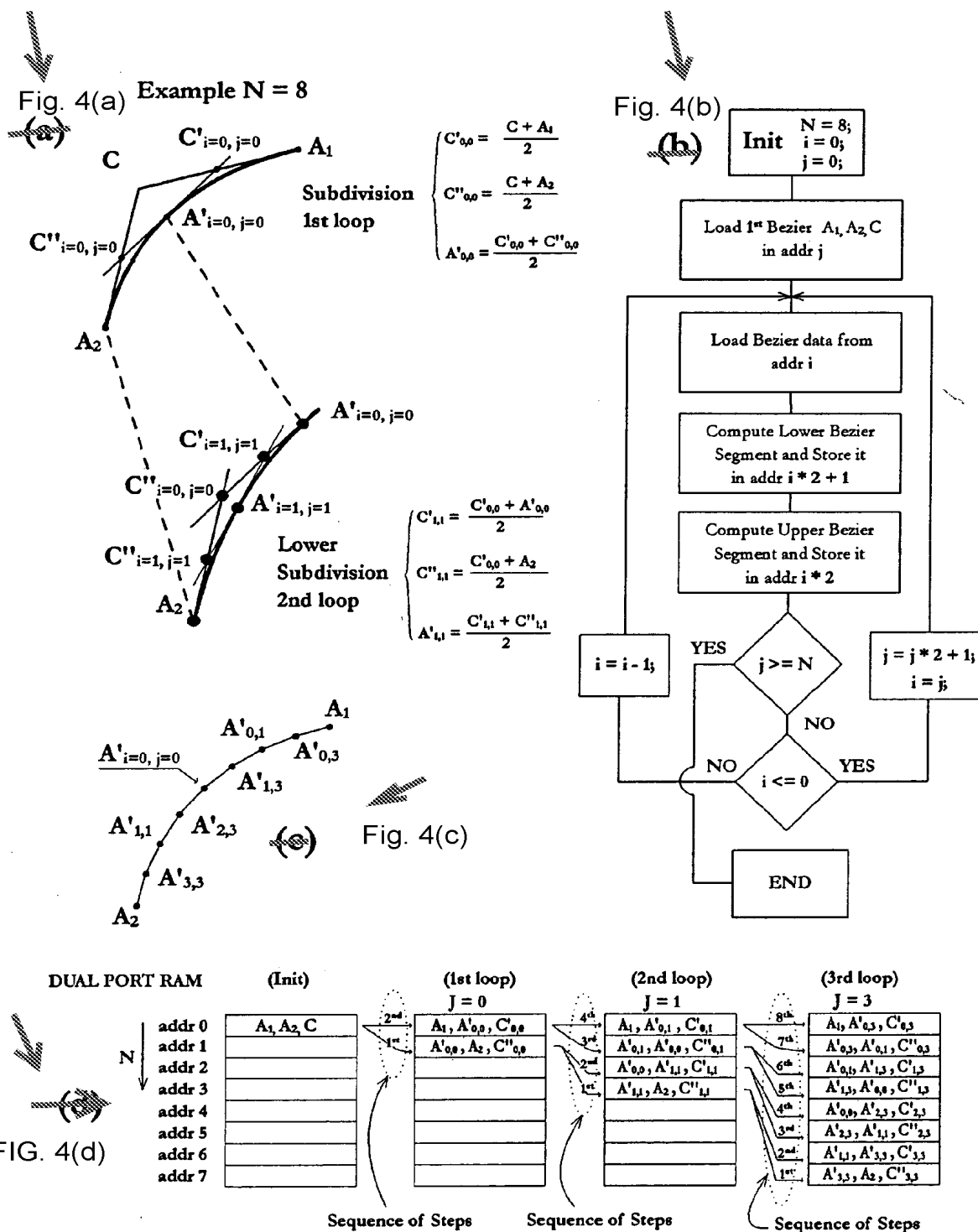


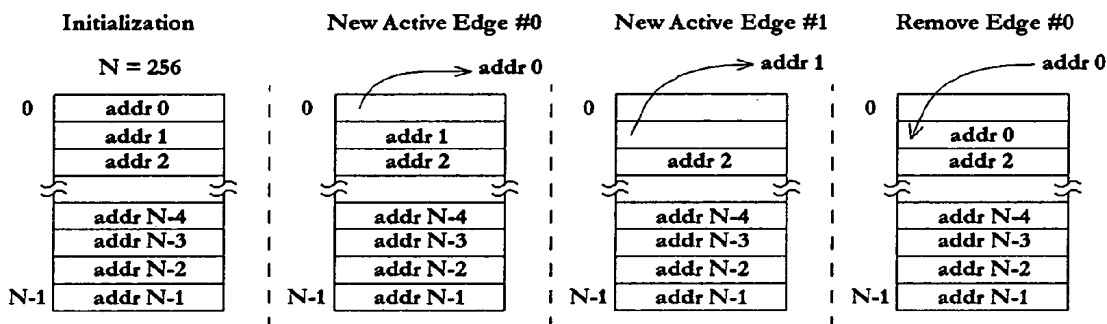
Strike FIG. 4

(a), (b), (c), (d), add FIG. 4(a), FIG. 4(b), FIG. 4(c), FIG. 4(d)



**FIG. 4**

Free Active Edge Stack (LIFO Stack Memory)



Strike (a)  
(b), (c), (d)  
& FIG. 5,  
add FIG 5(a)  
FIG. 5(b)  
FIG. 5(c)  
FIG. 5(d)

Active Edge Table: adding a new edge

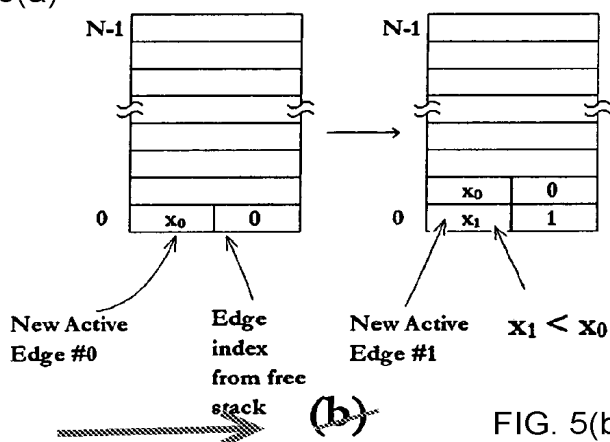
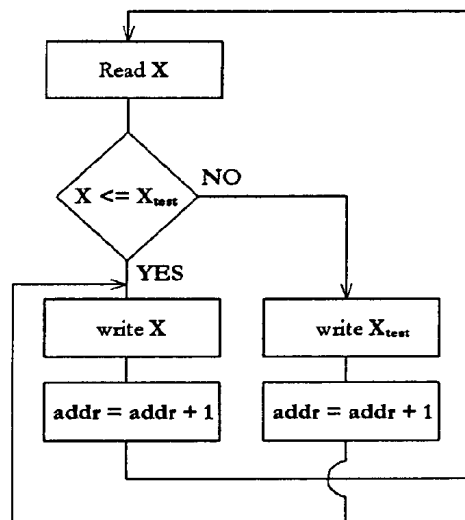


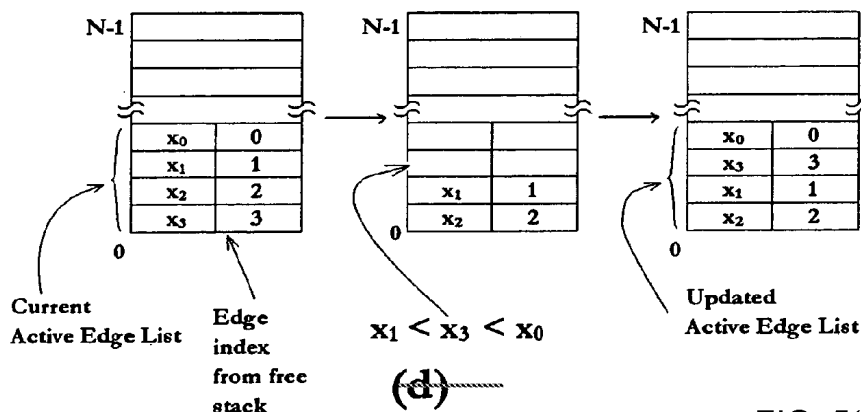
FIG. 5(b)



(c)

FIG. 5(c)

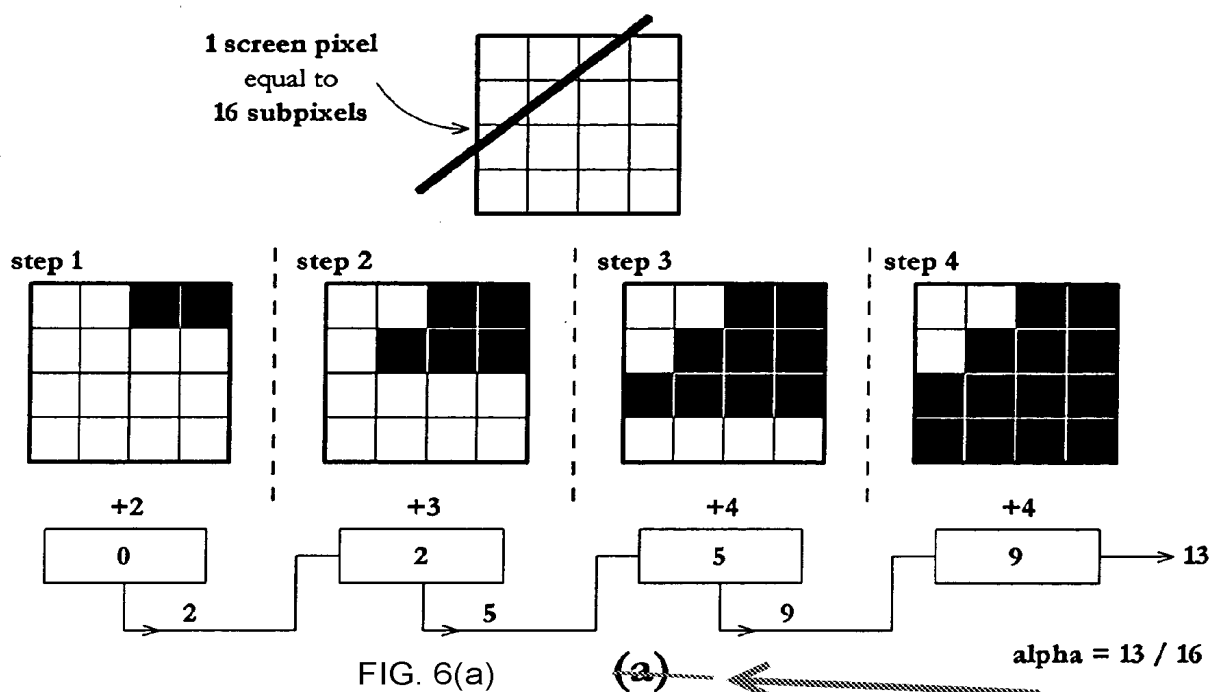
Active Edge Table: updating edge #3



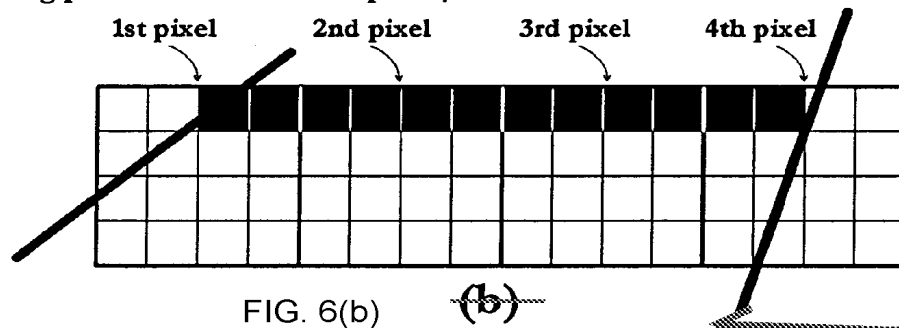
(d)

FIG. 5

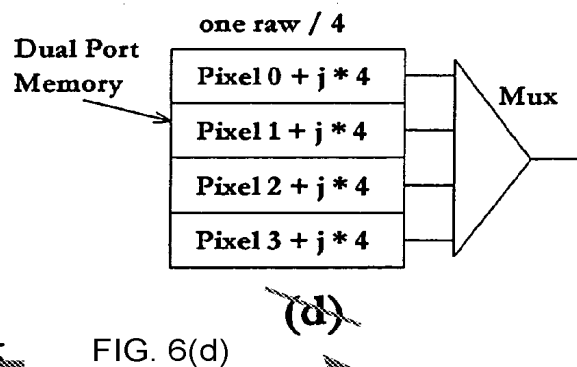
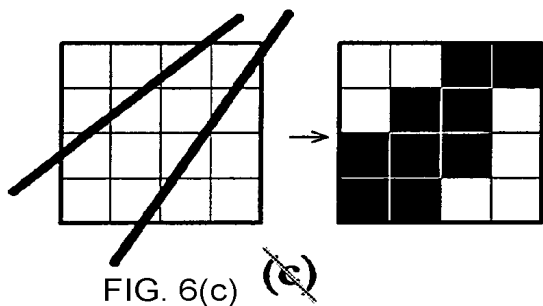
FIG. 5(d)



Anti aliasing parallelism with  $N = 4$  pixels;

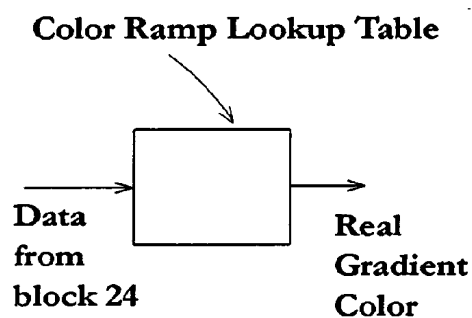
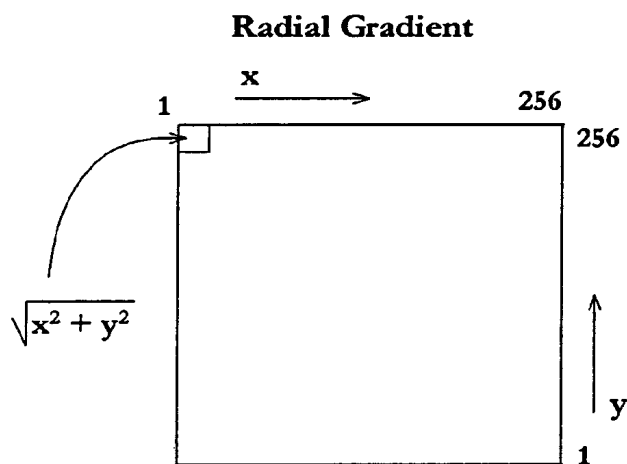
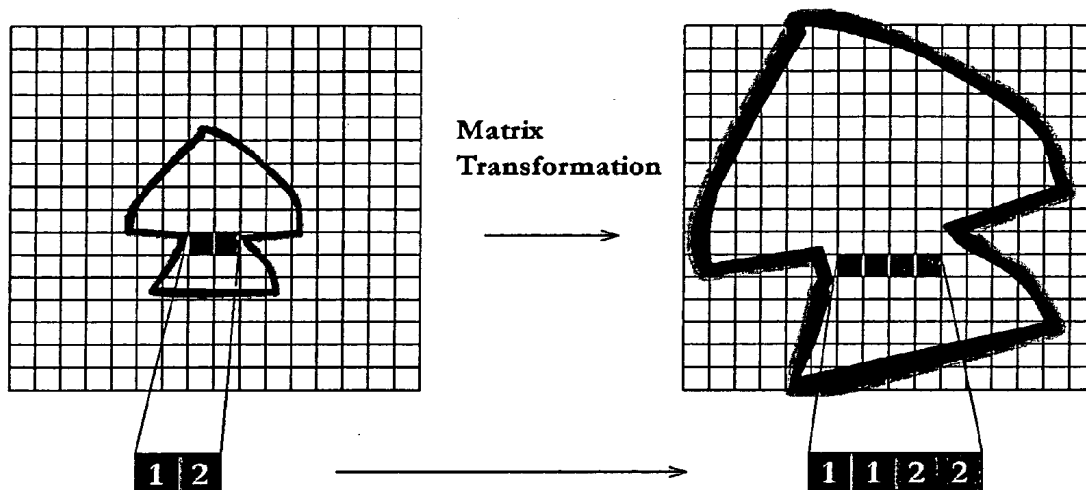


Init - End inside the same sub-pixel matrix



~~FIG. 6~~

Strike FIG. 6 and (a), (b), (c), (d)  
Add FIG. 6(a), FIG. 6(b), FIG. 6(c),  
FIG. 6(d)



~~FIG. 7~~

Strike FIG. 7, and (a), (b), (c), (d)  
Add FIG. 7(a), FIG. 7(b), FIG. 7(c), FIG. 7(d)

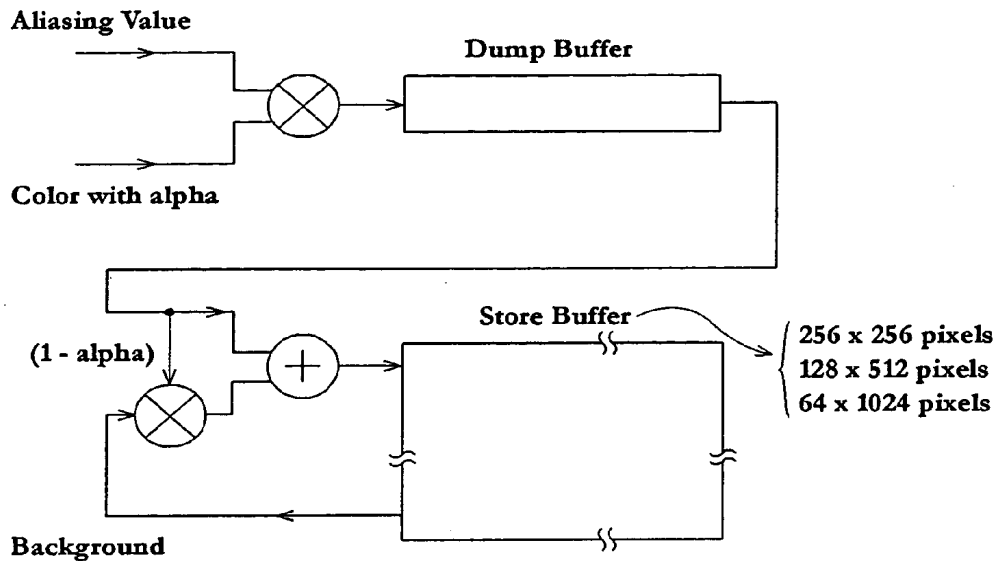


FIG. 8(a)

~~(a)~~

Strike (a) add FIG. 8(a)

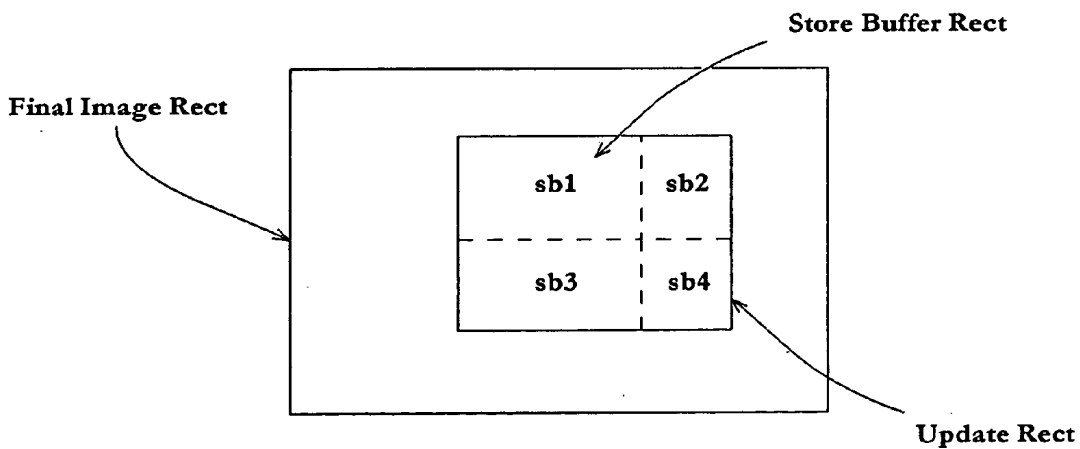


FIG. 8(b)

~~(b)~~

~~FIG. 8~~

Strike FIG. 8, and (a) and (b)  
Add FIG. 8(a) and FIG. 8(b)